IMPLEMENTATION OF DIGITAL SIGNAL PROCESSING (IDSP):

ORGANIZATION

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GOALS

• Becoming familiar with system-level issues relevant for the implementation of signal-processing algorithms.
• Knowledge of design flow and design automation tools.
• Becoming familiar with functional blocks typically used in implementations of signal processing (e.g. CORDIC, FFT)
• Becoming familiar with typical signal-processing algorithms as used in modern multimedia applications.
• Practical design experience.

RECOMMENDED KNOWLEDGE

• From the Master’s program:
  – System-on-Chip Design (191210750) or
  – System-on-Chip Design for Embedded Systems (191211590) or
  – Design of Digital Systems (192130022) or
  – Equivalent preparation with some basic knowledge of VHDL.

• Students without knowledge of System-on-Chip Design (for ES) will need to some reparation exercises costing about 10 to 20 hours.

• Knowledge of digital signal processing is convenient but not required.

1) Until September, mainly only present on Fridays

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PRE-KNOWLEDGE POLL

- A: SoC Design (for ES) & DDS (including 2021Q3)
- B: just SoC Design (for ES)
- C: just DDS (including 2021Q3)
- D: none of these

COURSE MATERIAL

- Not necessary to buy a book.
- Mainly journal articles, conference papers and book chapters distributed mostly through the course’s public web page with URL:
  http://sabihgerez.com/ut/vlsidsp/
- Material that is not linked via the page above, can be downloaded from the course's Canvas page.

LECTURES

- 7 lectures of (2 x 45 mins.) on Fridays 6th/7th hour (see WWW page for schedule details).

STUDY LOAD: 5 ECTS (140 hours)

- 7 lectures of 1.5 hours: about 10 hours.
- Studying the written material: about 30 hours.
- Practical projects and homework problems: about 100 hours.

HOMEWORK/PROJECT TEAMS

- To be performed in teams of two (rule), or alone (exception):
  - Sign up for teams on Canvas.
- Team members are supposed to contribute equally.
  - Contact instructor if you feel in disadvantage due to partner failing to contribute.
  - Signal problems in time, not just a few days before final deadline.
EXAMINATION

- Based on homework exercises, most likely involving Bibix tool Arx. Details to be published on public web page.

- All projects need to be completed by the end of quarter; see web page for exact dates.

- Students can propose alternatives for projects, especially for the larger final one.

SERVER ACCESS

- The exercises are to be performed on server xoc2.ewi.utwente.nl.
  - Login permissions need to be arranged for all students.
  - Enrollment data from Canvas/Osiris are used.
  - Late registrants should contact instructor.