# IMPLEMENTATION OF DIGITAL SIGNAL PROCESSING (IDSP):

#### **ORGANIZATION**

Sabih H. Gerez University of Twente Faculty of EEMCS Computer Architecture for Embedded Systems (EWI-CAES)

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## IMPLEMENTATION OF DIGITAL SIGNAL PROCESSING (191210950)

RESPONSIBLE GROUP:

IMPLEMENTATION OF DSP

University of Twente, Electrical Engineering, Mathematics and Computer Science, Chair for Computer Architecture for Embedded Systems (UT-EEMCS-CAES)

INSTRUCTOR:

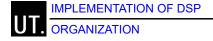
ORGANIZATION

Dr.ir. SABIH H. GEREZ<sup>1)</sup> (ROOM ZI 5033)

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1) mainly only present on Fridays

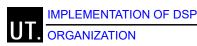
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#### **GOALS**

- Becoming familiar with system-level issues relevant for the implementation of *signal-processing algorithms*.
- Knowledge of design flow and design automation tools.
- Becoming familiar with functional blocks typically used in implementations of signal processing (e.g. CORDIC, FFT)
- Becoming familiar with typical signal-processing algorithms as used in modern multimedia applications.
- · Practical design experience.



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#### RECOMMENDED KNOWLEDGE

- From the Master's program:
  - System-on-Chip Design (191210750) or
  - System-on-Chip Design for Embedded Systems (191211590) or
  - Design of Digital Systems (192130022) or
  - Equivalent preparation with some basic knowledge of VHDL.
- Students without knowledge of System-on-Chip Design (for ES)
  will need to some reparation exercises costing about 10 to 20
  hours. See later.
- Knowledge of digital signal processing is convenient but not required.

#### PRE-KNOWLEDGE POLL

- · A: SoC Design (for ES) & DDS
- B: just SoC Design (for ES)
- · C: just DDS
- · D: none of these

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#### **COURSE MATERIAL**

- Not necessary to buy a book.
- Mainly journal articles, conference papers and book chapters distributed mostly through the course's public web page with **URL**:

http://sabihgerez.com/ut/vlsidsp/

Material that is not linked via the page above, can be downloaded from the course's Canvas page.

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#### **LECTURES**

• 7 or 8 lectures of (2 x 45 mins.) on Fridays 6<sup>th</sup>/7<sup>th</sup> hour (on one occasion 8th/9th hour, see WWW page for schedule details).

### STUDY LOAD: 5 ECTS (140 hours)

- 7 or 8 lectures of 1.5 hours: about 10 to 12 hours.
- Studying the written material: about 30 hours.
- Practical projects and homework problems: about 100 hours.



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## HOMEWORK/PROJECT TEAMS

- To be performed in teams of two (rule), or alone (exception):
  - Sign up for teams on Canvas.
- Team members are supposed to contribute equally.
  - Contact instructor if you feel in disadvantage due to partner failing to contribute.
  - Signal problems in time, not just a few days before final deadline.
- If you do not have a partner:
  - Come forward for matchmaking during the lecture break;
  - Sign up in special temporary Canvas group "Looking for a Partner".

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#### **EXAMINATION**

- Based on homework exercises, most likely involving Bibix tool Arx. Details to be published on public web page.
- First exercise to be released after 3<sup>rd</sup> lecture.
- All projects need to be completed by the end of quarter; exact dates to be published on web page.
- Students can propose alternatives for projects, especially for the larger final one.

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#### **SERVER ACCESS**

 The exercises are to be performed on server xoc2.ewi.utwente.nl.

- Login permissions need to be arranged for all students.
- Enrollment data from Canvas/Osiris are used.
- Late registrants should contact instructor.
- For issues related to server access (not those related to the contents of the exercises), please contact Dorus Abeln (d.m.abeln@utwente.nl).

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## (P)REPARATION EXERCISES

- Meant for students without knowledge of System-on-Chip Design (for ES).
- Students can start from Day 1; do not wait too long.
- · Not part of the examination.
- · No need to work in groups.